Amendments to the Specification:

Please replace the paragraph beginning on page 14, line 28, with the following rewritten paragraph:

The control-signal generator 72 includes a first OR circuit 180. The first OR circuit 180 outputs the clock-supply-control signal for common bus interface, based on OR condition between the request signal ~~43~~ 34 and an output signal 189 from a second OR circuit 188. The control-signal generator 72 also can include the second OR circuit 188. The second OR circuit 188 produces an output signal ~~190~~189, based on OR condition between the valid signal 54 and the BUSY information (signal) 50. The control-signal generator 72 includes a third OR circuit 182. The third OR circuit 182 produces the clock-supply-control signal 120 for dedicated bus interface for first semiconductor storage medium, based on OR condition between the request signal 43 and an output signal 191 from a first AND circuit 190. The control-signal generator 72 includes a fourth OR circuit 184. The fourth OR circuit 184 produces the clock-supply-control signal 130 for dedicated bus interface for second semiconductor storage medium, based on OR condition between the request signal 43 and an output signal 193 from a second AND circuit 192.